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IMPLEMENTATION OF LOW POWER MEMRISTOR CONTENT ADDRESSABLE MEMORY USING FINFET

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ABSTRACT

The research environment is promptly looking at the extensive development of memristor devices in industrial applications. Future technology is eagerly waiting for the upcoming developments in memristor-based devices. Memristor regulates the current flow in devices and the amount of previously flowed charges, which are stored as memory in applications. Any electronics design that employs computational technologies uses semiconductor memory. However, reading certain bits from the memory cell is time-consuming, while the same in the CMOS Content-Addressable Memories (CAM) zone is efficient. To overcome these limitations, a CMOS-Memristor Associative Memory Cell (MemCAM) is proposed, which is a multibit cell and merges the advantages of both memristor and CMOS logic. In Content Addressable Memory, the memories are not organized in chronological order and are associative. Non-volatile memory devices are getting popular in the era because of the developments in technology. Memristor memory devices acquired comparable features with existing memories like SRAM and DRAM, such as durability, consistency, and power compatibility with CMOS logic. Because each of the aforesaid memory devices has limitations, MEMCAM, a hybrid memory device, is used for improved data searching performance and reliability, as well as faster approaches. The integration of a FinFET-based circuit into the MemCAM structure enhances the efficiency and processing speed in various applications. This technique aims at the optimization of power dissipation with a tradeoff on area and analysis of characteristics like power consumption and delay, Noise Margin, and Frequency response. By combining the high-speed search capabilities of CMOS CAM with the low-power advantages of memristors and FinFET technology, this proposed system aims to develop hybrid memory architectures for next-generation computing systems, including artificial intelligence, machine learning, and high-performance processors.

Key words: *MemCAM, power dissipation, PDP, noise margin, and frequency response*

INTRODUCTION

The fast-paced and digitized existence of the early modern era has led to the introduction of large and complex datasets that must be handled quickly and rapidly. The faster data processing means faster data access wherever it's necessary. For storing and retrieving these data whenever necessary, memory modules are crucial. The limitations of scalability and leakage currents in memory devices based on CMOS are overcome by the memristor. [1]

The memristor is used mainly in Non-volatile memory applications, Computer technology, Logic circuits, Biological and neuromorphic systems, Digital circuits, and Digital and analogue memory. The cost is comparatively lower and is quicker than other devices like MRAM. The memristor can store a large amount of data and incur no information loss during the off-state. The information density of high importance is available, and due to less energy usage, heat production is less, and the data transfer rate is high [8]. Only a small amount of energy is used. This helps in the combination of one short device, hard drives, and working memory.[7]

In networking devices, CAM is frequently used to speed up forwarding information base and routing table operations. Cache memory also uses this technique of associative memory. CAM is one of the solutions for high speed. The CAM uses parallel active circuitry, which uses more power, and the primary aspect of designing it is to minimize power consumption without affecting speed or memory density [2], [13]. After the comparison of the needed information with the full list of information that is pre-stored concurrently, it outperforms alternative memory search methods such as binary or tree-based searches or look-aside tag buffers. This produces a reduction in the search time an order of magnitude. Memcam combines the advantages of both CAM and a memristor, thus allowing a more compact design. Memcam shows its benefits in the instruction and data caches in the on-chip caches. These are also manifested in the Translation Lookaside Buffer and the Branch Target Buffer [12].

This technique focuses on the optimization of power dissipation in a MemCAM device [10]. A memristor- CAM cell with Finfet is developed [4]. We have demonstrated the simulation on LT Spice. The evaluation of CAM parameters such as “Delay, Power Delay Product, and Noise Margin “is done, and the results are shown. The rest of the paper is organized as follows.

DESIGN PHASE

In contrast to CAMs, which just require a user to input a data word, the ordinary memory of the computer employs random-access memories (RAM), which require the address of the memory and the RAM to return the information stored at that place. For that data word, the CAM looks through its whole memory. If information was located, the CAM sends a collection of one or more storage addresses where it was identified. As a result, a CAM is the hardware equivalent of what software refers to as an associative array.

CAM is significantly faster than RAM in data search applications. However, CAM does come with some expenses. In a completely parallel CAM, each bit of memory has its similarity circuit to determine whether the stored bit and the input bit match. This is in contrast to a RAM chip that has cells that can store data in a simple manner. To give full information or data word match signal, the match outputs from each data word cell must also be concatenated.

The extra circuitry makes the CAM chip physically larger and more expensive to produce. The dissipation of power in the added circuitry becomes larger as the circuit that acts as the comparison is active in every clock cycle [6]. As a result, CAM is only used in situations where a less costly technique is unable to search as quickly. One early successful execution was a general-purpose associative processor IC and the system. Before employing content-addressable memory, high-speed searches were conducted using DRAM, SRAM, etc. DRAM is a memory device that stores data as bits based on metal oxide semiconductor technology. By storing 3 levels of voltage, we can reduce the overall power consumption. Instead of DRAM, low-power SRAMs can be used for other applications [20].

SRAM is a faster memory compared to dynamic random-access memory. SRAM uses a latching circuit, which often flip-flops to store data in its memory. Normal SRAM cells consume a large amount of power and their efficiency is lower. On the other hand, low-power SRAM cells can be used to overcome the power thirst of normal SRAM cells. When compared to the normal (or conventional) 6T SRAM cells, low-power SRAM cells use 38.1% less power. Low-power SRAM uses MTCMOS and gated VDD to reduce power consumption. These are the techniques added to the conventional 6T SRAM cell to produce low-power ones. When compared to the conventional ones, the MTCMOS-based SRAM cell is 18.18% faster. Also, gated VDD SRAM consumes 16.8% less power [5]. A memristor is an electronic device that is non-volatile and passive. In a memristor, the memristor state is shown as a logic value that is stored in the cell itself. This is one of the reasons why memristor is used for non-volatile memory storage. In high-density crossbar grids, memristors can be laid down; by using these devices, analog neuromorphic devices can be produced that can solve problems more efficiently. It's a type of passive storage element seen in flash storage, DRAM, and other devices. It is based on the applied electric field and a change in resistance. Conventional MOSFET technology may be replaced with FinFET technology to minimise power dissipation and increase the overall performance of digital logic circuits. FinFETs are the greatest choice as a MOSFET replacement below 32nm technology, because short-channel effects may cause more issues. FinFET technology has grown quite popular and widely utilised in practically all digital circuits due to its low leakage as well as low power features. FinFETs are multi-gate transistors with several gates that are built on a single device. The conducting channel of a FinFET is formed by a thin silicon sheet wrapped around the body[3].

Memristor

In the international research community of electrical and computer engineers, the memristor as a core constituent of the circuit has gotten a lot of attention. It is a passive storage element in flash memory, DRAM, and other applications. It works on the premise of applying an electric field to a resistance change. To prevent issues relating to sneak path, this requires that the resistance value does not change for the levels of voltage under a specific threshold. The Voltage Threshold Adaptive Memristor (VTEAM) model [21] exhibits sufficient accuracy (the largest relative RMS error was 1.48%) and computing efficiency based on this supposition. The equation shows the derivative of the state variable "m" of the VTEAM model. The parameter k_{off} is positive but k_{on} is negative since m is used as the breadth of the barrier when compared to prior models where the state variable was the width of the doped zones. [9]

Were,

$$\frac{dm(t)}{dt} = \begin{cases} k_{off}\left(\frac{v(t)}{v_{off}} - 1\right)^{\propto_{off}} f_{off}(m) & ;\ 0 < v_{off} < v \\ 0 & ;\ v_{on} < v < v_{off} \\ k_{on}\left(\frac{v(t)}{v_{on}} - 1\right)^{\propto_{on}} f_{on}(m) & ;\ v < v_{on} < 0 \end{cases} \quad (1)$$

m : is the width of the effective tunnel barrier

α_{off}, α_{on} : are model-fitting constants

v_{off}, v_{on} : are threshold voltages

f_{off}(m), f_{on}(m): window functions which confine m to the boundaries of m [mon, moff]

The implementation of the memristor was done in a software tool called LT Spice, and we have received the corresponding V-I Characteristics of the element.

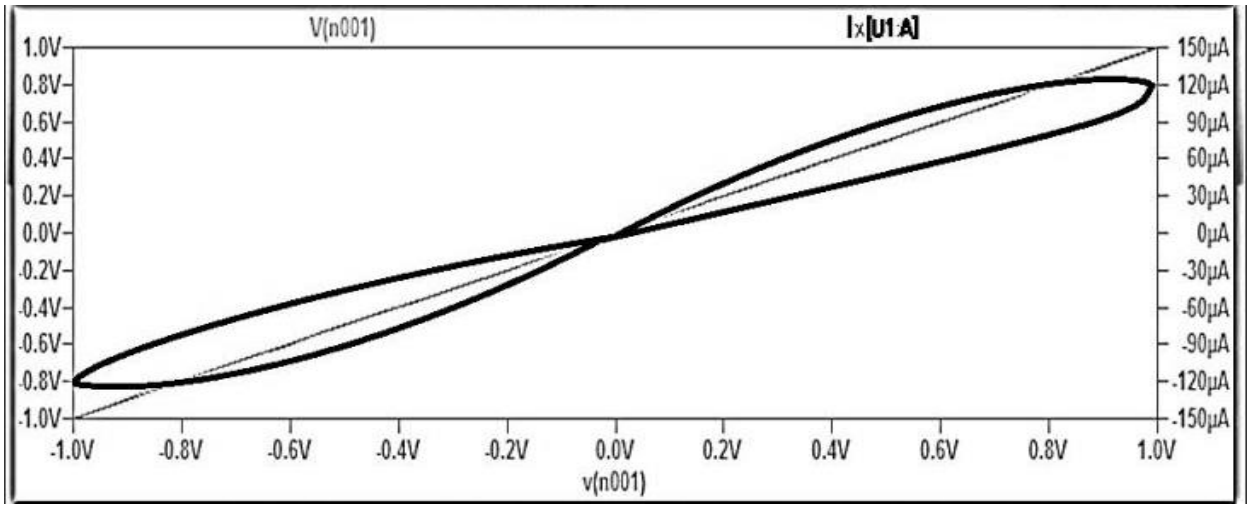

Figure 1. V I Characteristics of memristor

The characteristics of a Memristor are shown in the above Figure. 1, which has two curves- a Linear one and a nonlinear one. The nonlinear curve implies the hysteresis loop, which implies that the memristor is a dissipative element. If the frequency is increased, the loop gets suppressed. The linear curve/line indicates the applied DC voltage to the voltage across the memristor[16].

Type 1 Memristor Cell

The Type 1 memristor cell are 1-transistor 1-resistor memristor cell. The WL is enabled high for writing "1" and SL is grounded, the bit line is given some voltage, leading to an increase in voltage while the resistance drops, resulting in logic 0. The write and read operations are shown in Figure. 2.[14]

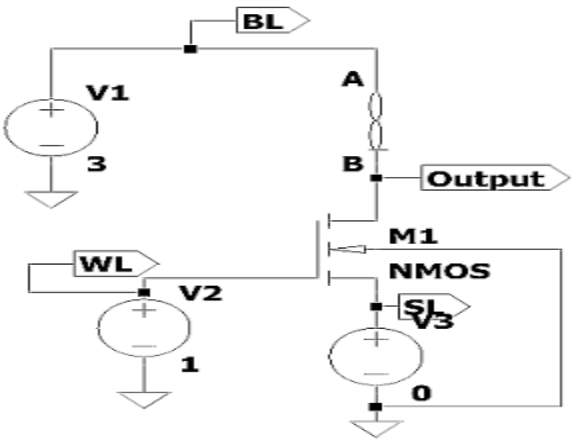

Figure 2. Write operation of type 1 memristor cell

In 1T1R, while writing "1", the memristor will store logic 1. So, if we give an input of 5V, and the resulting output will be approximately 5V. While writing, the BL will act as the input since it is across the memristor. Thus, the WL should be 1 to store the value and access it. While the write is enabled, the read must be disabled. This is the reason why WL is set high. Similarly, write "0". Below is the corresponding output for write 1 and write 0 [17].

Type 2 Memristor Cell

The Type 2 memristor cell is 2-transistor 1-resistor memristor cell. The current is regulated during the set operation of an n-type transistor in Type 1 by controlling directly the Gate-Source voltage. The high voltages that are being investigated will put a strain on the body.[18]

(i) the bit-cell transistor that has been chosen,

(ii) neighboring bit-cell selectors have the same BL and WL

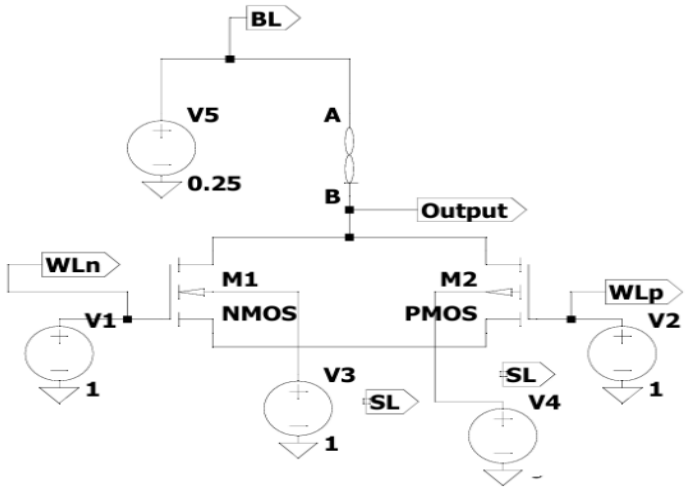

Figure 3. Write operation of type 2 memristor cell

A p-type transistor can be added to the Type 1 bit-cell to solve this problem, resulting in a Type 2 bit-cell. Only the n-type transistors are utilized in this architecture to regulate the current during the set operation (the p-type transistor gate-source voltage is kept zero). The p-type transistor is employed during the reset procedure. Source lines are used to control the set and reset operations. The WL_n and WL_p WordLines (WL_n and WL_p) are used to control the n and p-type transistors separately (Figure 3) [15].

Type 3 Memristor Cell

The Type 2 memristor cell are 2-transistor 1-resistor memristor cell in Figure. 4. In a Type 3 cell, the memristors are connected in series and are controlled by 2 transistors. For storing/writing the data to the memristor, WL should be turned high/on, and the source line should be given a minimum voltage so as to reset the system. The value to be stored in the memristor is fed to the bit line. The corresponding output should be taken across the memristors. From the graph, it is seen that both the memristors store the same value when a low input is fed [19].

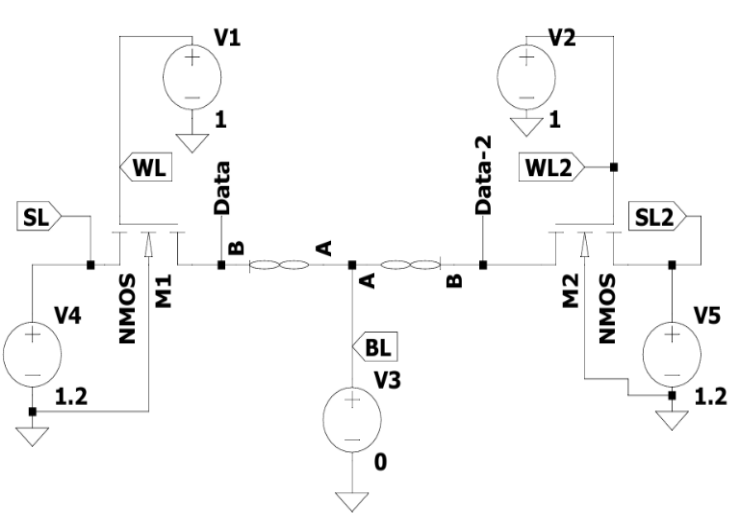

Figure 4. Write operation of type 3 memristor cell

PROPOSED DESIGN

MemCAM

The MemCAM device combines CMOS memory's speed and simplicity of search with the scalability of memristor memory. Memristor devices are used instead of CMOS-based devices since CMOS-based devices have limited scalability due to problems with their leakage current and static power consumption. Memristors store information by changing their resistance state, and this information is stored when switched off, thus they use no static power. Thus, memristive devices are offered as a possible alternative because of their ultra-high density and power efficiency. The crossbar structure, in which a memristor is introduced at each crosspoint, is the most scalable when we consider all the memristive memories.

Memristors are also used in content-addressable memories. MemCAM has a hybridization scheme, different from earlier CAMs with memristors that employed two memristors in place of the latch and a conventional CAM cell, which has a crossbar of memristors on top to boost capacity, used for operations such as write, read, and search. Consequently, one cell contains a typical CMOS memory cell along with several memristors (based on the crossbar size). MemCAM is a CMOS binary CAM cell based on memristors that uses multiple bits with a cell of SRAM that improves performance and utility while remaining competitive with existing CAMs [11]. The function of control signals whenever data is stored in the memristor and read out from the sense amplifiers is described in Figure. 5.

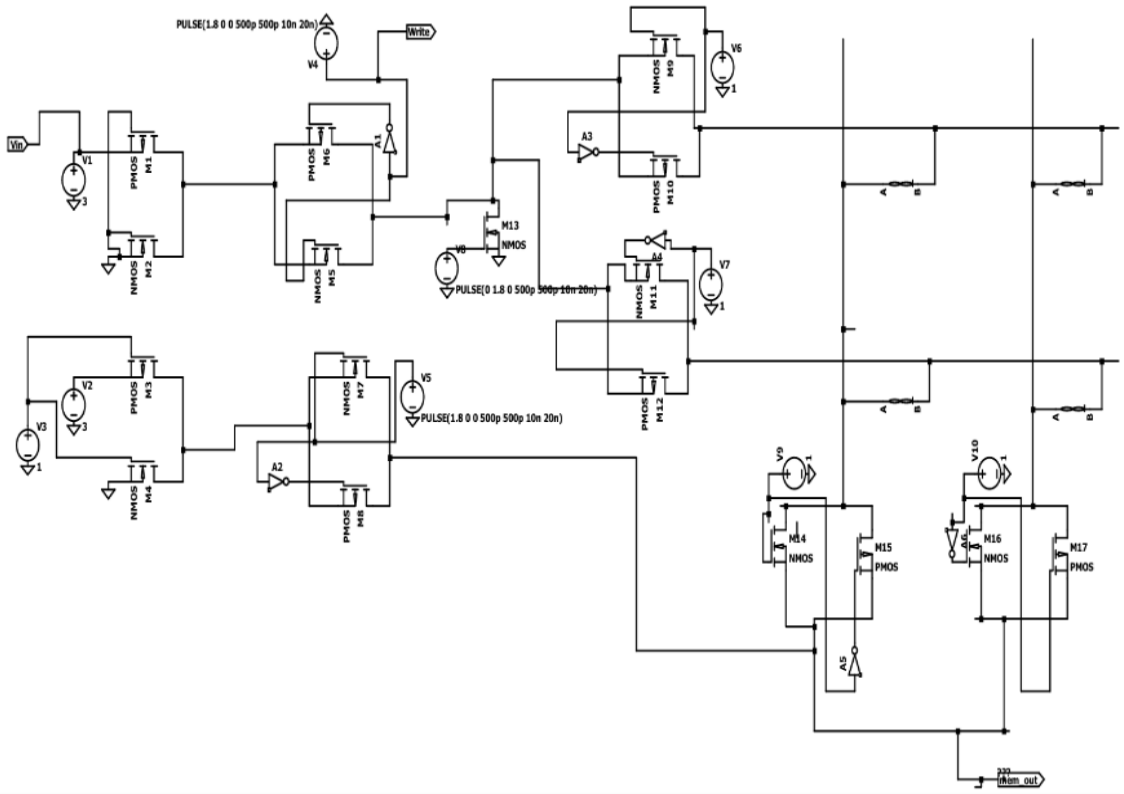

Figure 5. MemCAM circuit

A. MemCAM with FinFET

Optimization is key to maintaining a better design since it boosts productivity and efficiency. Cascaded double-gated shorted FinFETs are used in the presented design paradigm. The Write signal is activated throughout the write cycle, while the Read signal is disabled, and the data is stored in the memristor. The reverse occurs during the read cycle. The signals are sent to the read circuitry and subsequently to the sense amplifier via the mem_out nodal voltage. To store and read data, the design has replaced the

memristor with a memristor-based FinFET. A typical voltage sense amplifier is also used to establish the output. The memristor-based FinFET will be able to receive both lower and higher voltages due to the transmission gates [22]. Figure. 6 shows how the voltage levels vary in concept.

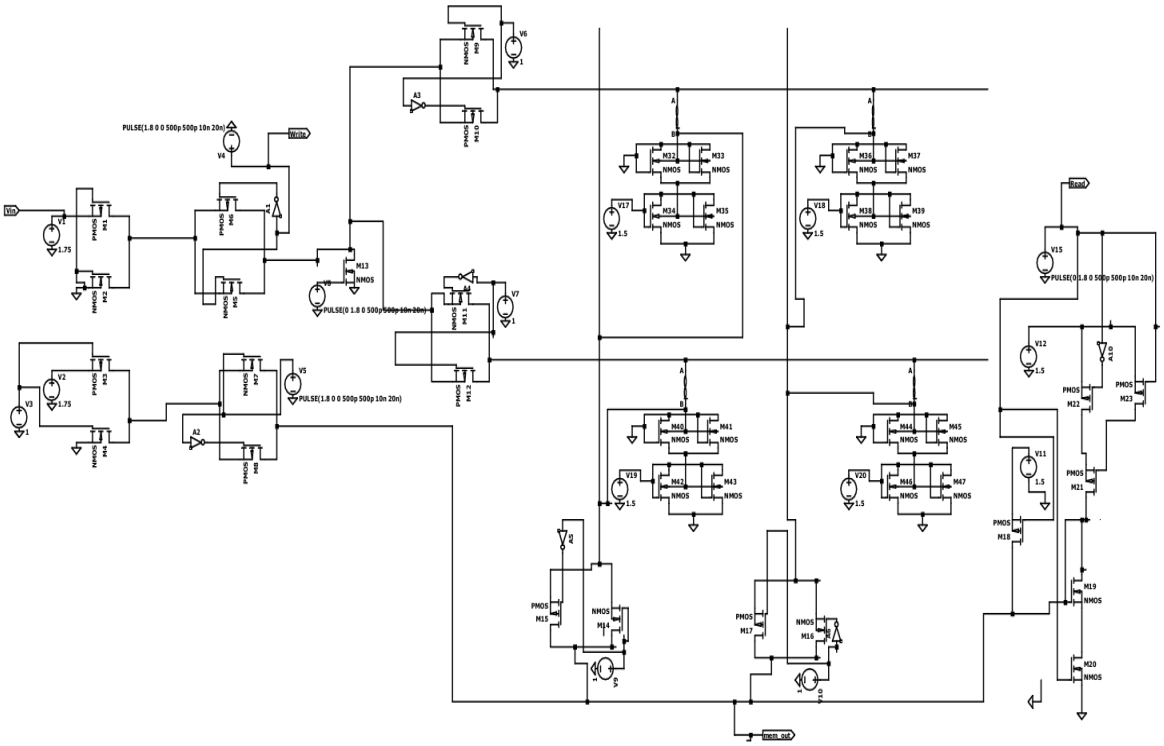

Figure 6. MemCAM with FinFET circuit

The voltage level is sent to the memristor through the select lines, and the output is designated by Vout. Because both the gate and the drain are shorted, the gate may regulate the channel length more effectively than a MOSFET. The electric field is used by the FET to modulate the conductivity via the channel. The gate voltage regulates the channel length, lowering the leakage current. The change in the voltage provided to the FinFET and the output voltage, which is in the millivolt range, may be seen in Figure. 7

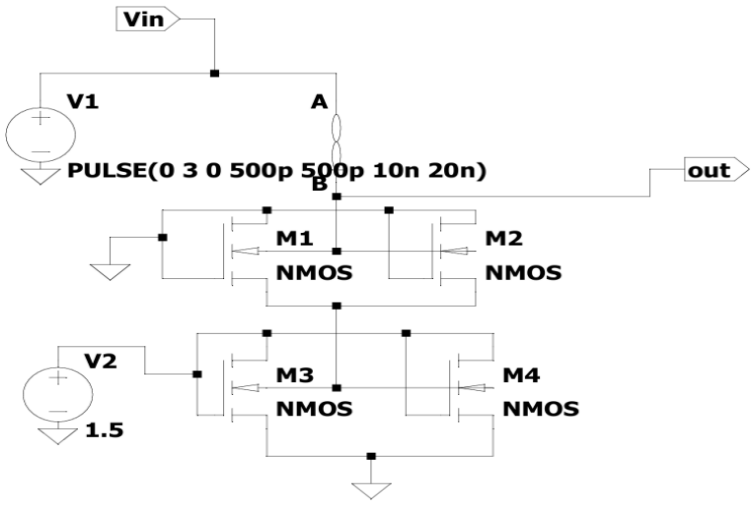

Figure 7. Short gated FinFET device

The sense amplifier (Figure. 8) is the last part that works in two stages, i) precharge and ii) evaluation stage. The bit line and Bitline Bar voltages from the read circuitry are supplied to the differential input

stage by transistors M55-M56. The differential input stage increases the difference between the differential interconnect's input signals. The cross-coupled inverter is made up of transistors M49-M53. M54 is an equalization transistor that is used to shorten the sensing amplifier's aperture time.

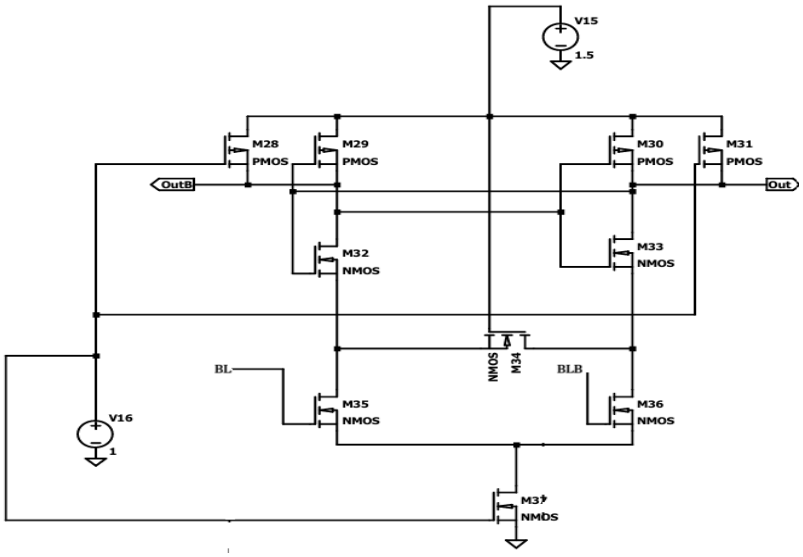

Figure 8. Conventional voltage sense amplifier

The gate voltages of M48, M51, and M57 are clocked to regulate the circuit. Through M48 and M51, all internal nodes are pre-charged to a high level during the clock's low phase. M57 is turned on by the positive edge, which starts the evaluation phase and produces the tail current. The sense-amplifier identifies the voltage of the input and latches the converse to the output during the evaluation phase. M55 and M56 are the input pairs that convert a differential input voltage to a differential current. The current differential between the two sides of the load and the resulting charge imbalance at M52 and M53's source nodes (also known as the "sense nodes") causes one of the output nodes to decrease quickly than the other. The output is given positive feedback by the cross-coupled inverters. The bit line and Bitline Bar voltages are fed to the sense amplifier's input. The corresponding output obtained in the sense amplifier is shown in Figure. 8.

RESULTS AND OBSERVATIONS

Experimental Results

The graphical simulation of Type 1 is shown in Figure. 9. When a high input is stored across the memristor, a near-high level output is generated.

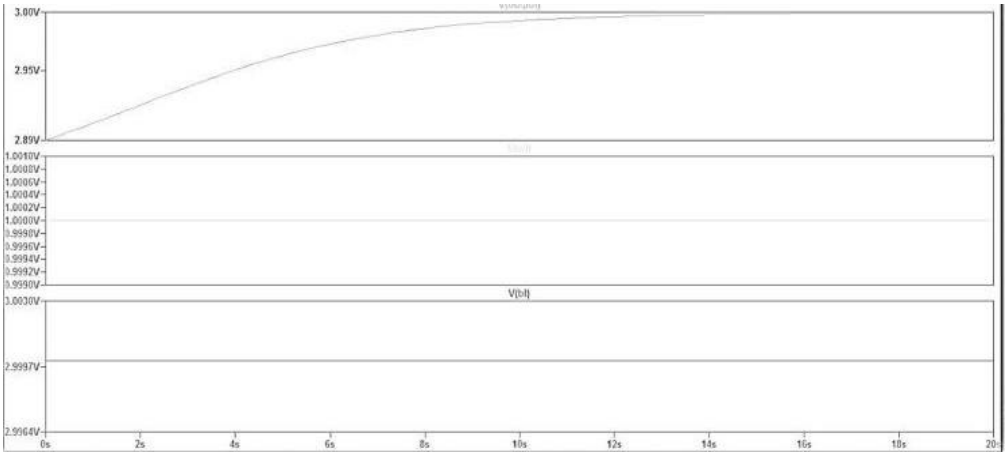

Figure 9. Simulation of type 1

The graphical simulation of Type 2 is shown in Figure. 10. When a high input voltage is provided to the memristor, the output voltage varies as shown in Figure. 10. It employs two transistors that are controlled by source line voltages.

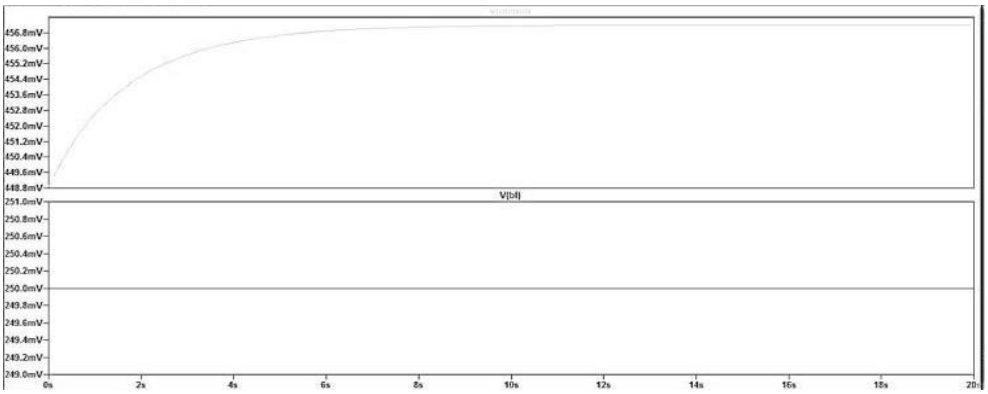

Figure 10. Simulation of type 2

The graphical simulation of the 2t2r write cell is shown in Figure. 11. The bitline voltage indicates the input voltage that is needed to be stored in the memristor. The output data from the memristor is also logic low as indicated from the graph.

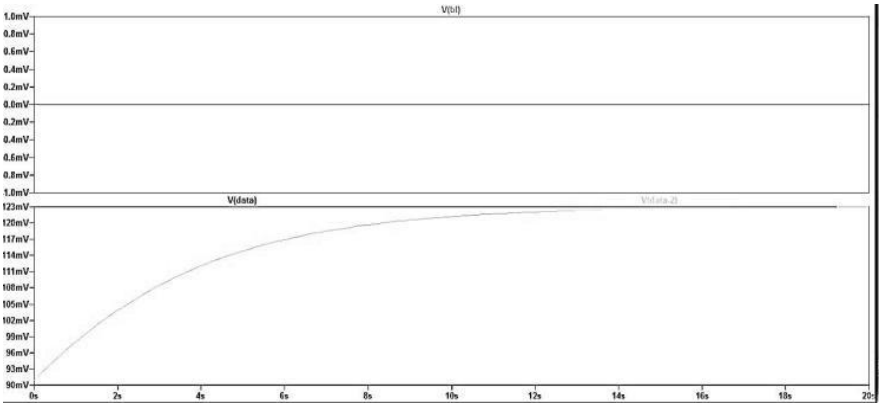

Figure 11. Simulation of type 3

The graphical simulation of the MemCAM circuit is shown in Figure. 12. The data written to the memristor and read from the memristor are shown in the graph above, with the write and read signals for the high inputs enabled.

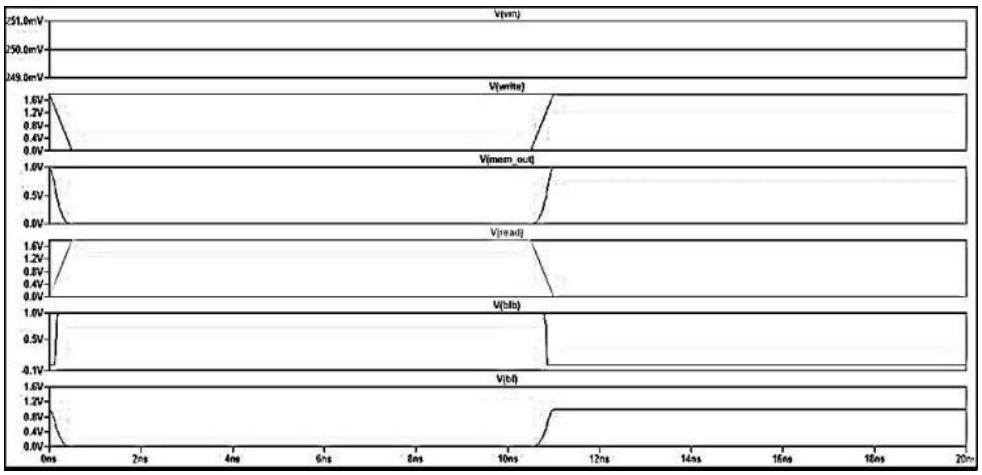

Figure 12. MemCAM stimulations (low input)

Figure. 13 shows the data written to the memristor and read from the memristor, with the write and read signals for the high inputs enabled. However, there's a change in the voltage stored in the memristor.

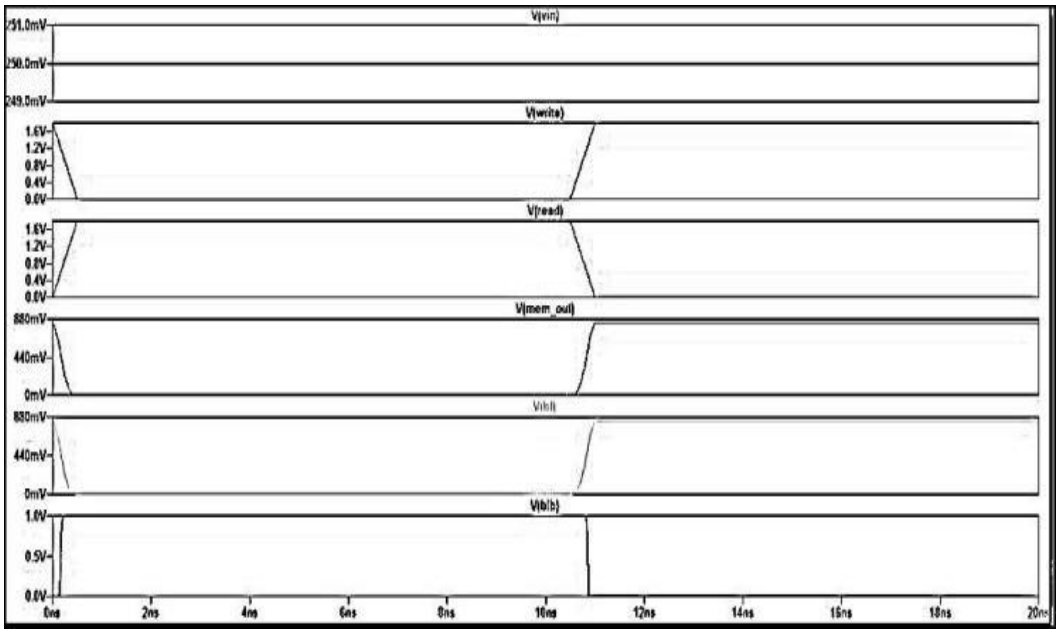

Figure 13. MemCAM with FinFET simulations (low input)

The graphical simulation of the FinFET Circuit is shown in Figure. 14. It depicts how the output voltage changes when a specific input voltage is applied. The output voltage of the FinFET has been reduced, and the simulation also shows the current flowing through the memristor.

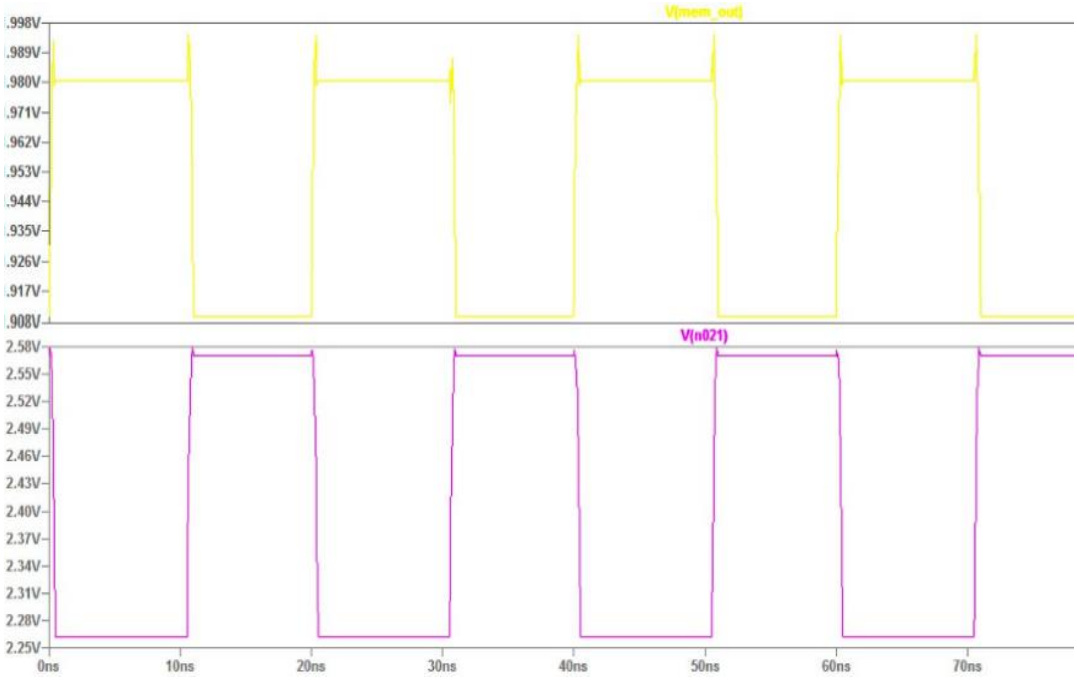

Figure 14. Simulation of FinFET output

It is evident from Figure. 15 that in the proposed design, the bit line voltage is greater than the bit line bar, indicating that the bit line voltage is logic high.[23]

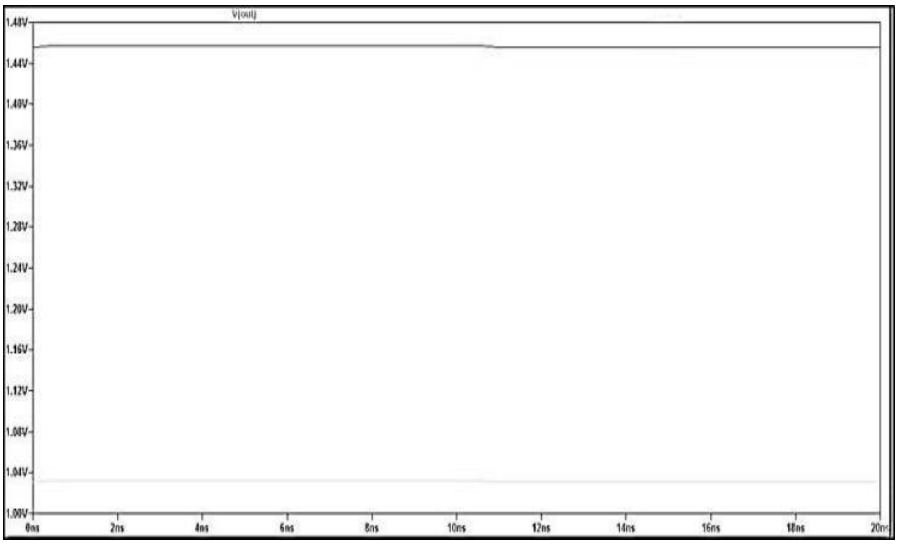

Figure 15. Sense amplifier output (high input design)

RESULTS AND DISCUSSION

Power dissipation

In Write 0 and Read 0, we assume low voltage near logic 0 as the input voltage, and the corresponding output is taken from the Mem_{out} for Write 0 and from the bit line for Read 0, MemCAM, and the proposed design. In the case of Write 1 and Read 1, we assume high voltage as the input voltage, and the corresponding output is taken from the Mem_{out} for write 0 and from the bit line for Read 0 of MemCAM and of the proposed design. For Write 0 and Write 1, the corresponding voltage within that node and the current passing through that node are taken, and their product is calculated to get the power dissipation of the corresponding circuits. For Read 0 and Read 1, the corresponding bit line voltage and the drain current of the nearest MOSFET are measured, and their product is measured to get the power dissipation. Table 1 shows the power dissipated during read and write operations in MemCAm and the modified structure of MemCAm with FinFET.

Table 1. Comparison Of Power Dissipation

Power dissipation	**Comparison**	
	MemCAM	***MemCAM with FinFET***
Write-0	1.26uW	1.02uW
Write-1	20.73uW	15.74uW
Read-0	0.0014fW	0.00017fW
Read-1	0.0196fW	0.0054fW

Delay

The propagation delay (t_P) is defined as the average of the low-to-high (t_{PLH}) and the high-to-low (t_{PHL}) propagation delays. Propagation delays t_{PLH} and t_{PHL} are the times needed for the voltage at the output to reach the centre between the low and high logic levels, i.e., 50 % of VDD in the case of CMOS logic.

$$t_P = \frac{t_{PLH} + t_{PHL}}{2} \quad (2)$$

The estimated propagation delay from the simulation is shown below in Figure. 16. For the proposed design, the write delay is defined as the time taken for the memristors to store the data when the write signal is enabled. Also, the read delay is defined as the time taken for the output across the memristor to be read from the bit line when the read signal is enabled.

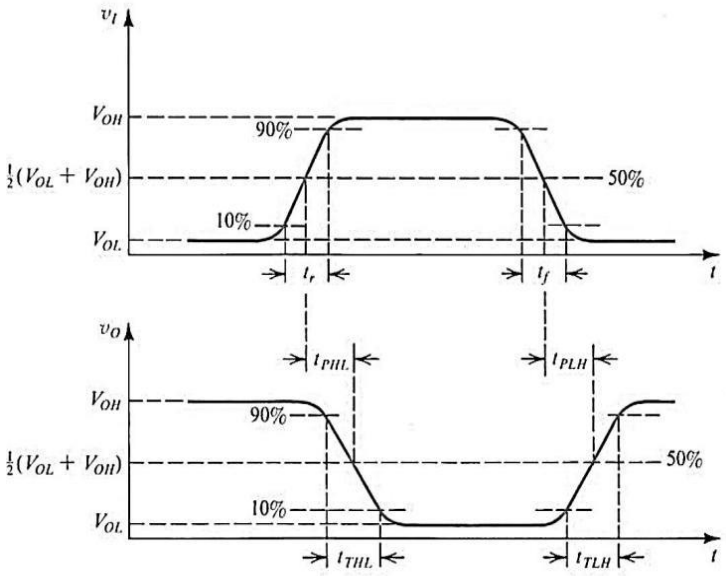

Figure 16. Estimation of propagation delay using the graphical method

Table 2 and 3 show the write and read delay associated with MemCAm and MemCAm with FinFET structure. A drastic decrease can be observed in the MemCAm with FinFET structure.

Table 2. Comparison of write delay

Write delay(nS)	**Comparison**	
	MemCAM	***MemCAM with FinFET***
Logic-0	0.098	0.030
Logic-1	0.044	0.0231

Table 3. Comparison of read delay

Read Delay (pS)	**Comparison**	
	MemCAM	**MemCAM with FinFET**
Logic-0	106.62	15.22
Logic-1	107.5	15

Noise Margin

The noise margin is the quantity by which a wave is above a certain value for a correct '0' or '1' in a digital circuit. A digital circuit, for example, may be constructed to differ from 0.0 to 1.2 volts, with any value less than 0.2 volts being a '0' and above 1.0 volts being a '1'. Table 4 shows the static noise margin of MemCAM and MemCAM with FinFET structure. It is obvious that the static noise margin associated with the MemCAM with FinFET is significantly lower than that of the MemCAM structure.

Table 4. Comparison Of Noise Margin

Static Noise Margin(V)	**Comparison**	
	MemCAM	***MemCAM with FinFET***
SNML	1.03	**0.24**
SNMH	-1	**0.13**

Power Delay Product

Table 5 contains the comparison of the Power Delay Product of MemCAM and MemCAM with FinFET. Power Delay Product is the product of the power dissipated and the propagation delay. The results show the PDP associated with the MemCAM, FinFET is lower as compared to the MemCAM structure.

Table 5. Comparison of Power Delay Product

Power Delay Product(fJ)	**Comparison**	
	MemCAM	***MemCAM with FinFET***
Write-0	0.123	0.0306
Write-1	0.912	0.363
Read-0	1.49*10^-13	0.025*10^-13
Read-1	21.07*10^-13	0.81*10^-13

CONCLUSION

The proposed circuit is a novel low-power memristor content-addressable memory using FinFET. The structure is that of memristor-based content addressable memory with the addition of a double-gated cascaded FinFET at the output of the memristor devices. The proposed design enables the memristor-based CAM to have low power dissipation, at the same time, no trade-off in its performance is required. The implementation of the above-mentioned is presented, along with which the calculation of write delay, read delay, noise margin, and power delay product is also done. After the implementation of the proposed design, the power dissipation for write-0, write-1, read-0, and read-1 was reduced by 19.04%, 24.07%, 87.85%, and 72.44% respectively. For logic-0 and logic-1, the write delay is reduced by 69.38% and 47.50% and the read delay for logic-0 and logic-1 is 85.70% and 86.04% respectively. Power Delay Product, along with Noise Margin, for the design was also reduced.

Availability of data and materials

The authors confirm that the data supporting the findings of this study are available within the article and its supplementary materials.

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