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OPTIMIZED RESISTIVE RAM USING 2T2R CELL AND IT'S ARRAY PERFORMANCE COMPARISON WITH OTHER CELLS

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SUMMARY

In the contemporary context, non-volatile-based Resistive Random-Access Memory devices are one of the most promising and emerging technologies. It is one of the top alternatives for industrialists since they are considered to offer neuromorphic in-computing capacity. This study aims to build a 2T2R RRAM cell with reduced power dissipation compared to various RRAM and SRAM cells. The Project used Cadence Virtuoso to simulate in 90nm Technology. The proposed 2T2R structure and analyze the elements that lead to power dissipation for various optimizations. The results demonstrate that RRAM has an effective PDP which is less than most modified SRAM techniques. Furthermore, compared to RRAM cells, 2T2R is the most efficient in power dissipation, PDP, and Noise margin. A technique for reducing the power and delay has been proposed and which resulted a drastic reduction in power, delay, and PDP of the modified circuit respectively. The 2T2R circuit thus incorporated into a 4*4 array matrix which has an optimized power dissipation. As a result, the purpose of the research is to demonstrate that the RRAM cell outperforms the existing memory technologies and the 2T2R RRAM Cell and its memory array is the most stable cell and shows increased read and write performance, stability, and energy efficient.

Key words: *RRAM, power reduction, stability, circuit design, noise margin, PDP.*

INTRODUCTION

The present semiconductor memory technology is a storage device that is built on a semiconductor-based computer circuit that is currently quite basic in the industry. New and improved semiconductor memory technologies are being investigated in response to the rapid development in the demand for semiconductors. Older semiconductor memory technologies are still in widespread use and are expected to do so for several more years. Memory is frequently divided into two types: volatile and nonvolatile. Nonvolatile memory, also known as secondary memory technology, does not lose its data even when the facility is switched off, whereas volatile memory loses its contents if power is shifted and preserves the information until the device power is turned on. Read-Only Memory (ROM), in which data is written

once and can be read repeatedly, whereas Random Access Memory (RAM), in which reading and writing of information can often be done in any order, and Flash Memory, in which data is written and erased in blocks, are the most researched and established semiconductor memory technologies [1][4]. Each one can be further categorized and has its own set of benefits and applications.

Since the nonvolatile memories can preserve data when the power is turned off, as the technology improves the interest in deploying these types of memories in several forms will increase gradually. Hence memory arrays are being utilized which are energy efficient and extremely precise. Large connection networks in FPGAs and neuromorphic systems demand high-capacity memory arrays, which are typically utilized to build speedy but reduced power crossbar modules. To boost the computing performance of the system and energy efficiency, researchers have emphasized CMOS technology devices and the far side of von Neumann architectures [19].

Memory technologies mix the benefits and drawbacks to improve performance. DRAMs in a computer, for example, have a lot of capacity and density, and they are also volatile, which means they need to be refreshed every few milliseconds. As a result of this refreshing, the device's energy consumption will increase, which isn't ideal. SRAM, on the other hand, is larger, making it more difficult to use on a bigger scale [10]. Flash memories, which include MOSFETs and a floating gate within every memory cell, are increasingly widely utilized for embedded related applications because of their high density and relatively less expensive [3].

The three memory technologies listed above, SRAM, DRAM, and Flash, are all charge storing memories. Here, DRAM uses charge storage at the capacitor to store data, SRAM uses charge storage at the nodes of inverters that are placed cross-coupled to store data, and flash memory uses charge storage at the floating gate of the semiconductor device. All of these charge storing-based memory technologies are having trouble scaling down towards 10-nanometer nodes or even above that. This is commonly linked to the reduction of stored charges at the nanoscale, which leads to a drop in performance, dependability, and noise margin [18]. Furthermore, DRAM necessitates a large amount of refresh dynamic power, and each SRAM necessitates a large amount of leakage power. DRAM also poses considerable challenges when it comes to memory hierarchy design in the future.

As a result, the term "emerging memory" is frequently used to refer to different sorts of memories. Hence RRAM (Resistive random-access memory) is a nonvolatile memory choice over the next-generation memory storage. RRAM memory devices are appealing because of their small size, minimal programming voltage, quick shift speed, and easier integration with CMOS fabrication technology [13].

This paper is organized as follows: Section 2 discusses existing memory architectures and approaches, while Section 3 provides a quick overview of memristor modeling technology. Section 4 delves into the design and operation of RRAM array structure, while Section 5 explores the non-volatile memory activities in depth and finishes the simulation results and inferences. Finally, Section 6 concludes the paper.

EXISTING MEMORY CELLS

In this section below, some findings on the existing and emerging memory technologies are briefly discussed.

Memory technologies are important in the growth of technology and the evolution of more devices in the nanoscale range and beyond. When devices are scaled-down, the problem of power dissipation increases, making the system unstable and resulting in poor performance. As a result, power optimization is currently a prominent topic among researchers [7]. The most prevalent technology for storing charge in the form of cross-coupled inverters is static random-access memory. A 9T stable structure that optimizes power, delay, and power delay product due to several shortcomings in previous 6T SRAM designs is proposed [5]. When compared to a typical 6T SRAM design, the suggested system is said to save 62.273 percent on power. In comparison to previous 6T designs, there is a 66.6033 percent reduction in PDP. As a result, the proposed structure is thought to be more stable and perform better.

Memory arrays based on CMOS architecture and the existing memory technologies are currently experiencing numerous hurdles in terms of reducing power consumption and delay [2]. As a result, in the current circumstance, different external supplemental technologies are being investigated. Memristor technology, which uses resistive switching to overcome the problem of power dissipation, is a new potential option [16]. In this literature, a one-transistor one memristor Resistive RAM Model is simulated in Cadence Software, and the simulations are illustrated [6]. The results show that the time required to write the logic "1" value is 30 percent longer than the time necessary to write logic "0." Another significant element considered in the research was energy dissipation, which was nearly the same in both cases of writing "0" and "1." When reading, the energy expended was roughly 120fJ/bit, which was roughly 65 percent less than when writing.

The metal-oxide-based non-volatile RRAM is a new memory technology that is gaining traction. RRAM's unique ability to perform digital, analog, or arithmetic logic has permitted it to combine computing and memory features in one device. Because of this intriguing trait, there has been a growing tendency to use RRAM structures to create new intensive data algorithms in recent years. A standard resistive RAM-based computation architecture might have lot more RRAM units called mats that could store or process information. In this study, a scalability network-on-Resistive RAM architecture to accommodate such a massive scale RRAM topology is presented [20]. The proposed network makes use of a unique associative routing design relying on content-addressable memories based on resistive ram technology. The routers deliver superior throughput and optimization of resources than a traditional router because of their in-memory-based packet processing capabilities. This router is RRAM-compatible, and their tests demonstrate that using it to create a network-on-RRAM makes upcoming RRAM-based computation architecture more extensible and performance-efficient.

Single-event upsets occur when the impacting particles' energy is sufficient enough to directly change the memory cell's data from High Resistance State (HRS) to Low Resistance State (LRS) or vice versa. Numerous strikes are required to entirely switch the logic data stored in the memory cell from one state to the other in the case of intervening alterations in the backup repository of the 1 Transistor 1 Resistor (1T1R) cell. Multiple-event upsets are the term used to describe these soft errors. This study explores a unique methodology for identifying and then fixing Single Event Upset (SEU) in a (1T1R) Resistive switching memory array, which can be easily integrated in other memory applications. The suggested solution involves adding an extra RRAM device to the cell structure and altering the read and write operations accordingly. Hence, a solution in the 1T1R array for Single Event Upset which incorporated a new method to modify the read and write functions respectively is proposed [8]. All the proposed solutions may increase the energy consumption of read/write operations by just +0.2% and +0.1%, respectively, for an 8-Gb 1T1R memory array, according to the results of SPICE simulation.

Computation in memory (CIM) using nonvolatile memories (NVM) is a potential alternative for intensive data scenarios. Here, an RRAM has a 2T2R (2 transistors and 1 Resistor) cell architecture that enables three CIM functions: A) Arithmetic operations blocks and logic in-memory or LiM primitives; B) ternary content addressable memory (TCAM); C) in-memory dot-product utilized for neural networks is presented [9]. The studies show that the conventional 1T1R and 2T2R configurations are both supported by the proposed design. When compared to the conventional LiM-Full adders, the suggested LiM full adder helps in the reduction of the static power, and dynamic power, and hence the delay by1.6%, 1.2%, and 0.6% respectively. In comparison with the state-of-art LiM-FA, the suggested LiM-FA enhances the delay (3.2%), static power (1.2%), and dynamic power (1.6%). The same VREAD for the RRAM access could be established in 2T2R and 1T1R setups using optimizations and robustness analyses. In a 1T1R cell architecture, a lower VREAD results in 1.14% reduced access energy.

MEMRISTOR MODELLING TECHNOLOGY

Memristors were predicted in 1971 and later considered the fourth important element, following resistors, capacitors, and inductors. Memristors are said to directly link magnetic flux and charge. The memristor has the unique virtue of being able to adjust its resistance value by providing a sufficient voltage drop across the terminal plates, and hence the resistance value remains constant even when the voltage is removed. As a result of resistance switching, a pinched hysteresis loop can be seen in the current-voltage

characteristics of a memristor. Following that, numerous other research groups were successful in fabricating devices with similar features. Memristors have several distinct benefits over ordinary MOS transistors, one of which is their incredibly small size. A memristor with a feature size of 9 nm2 may be manufactured. Memristors can be used to make high-capacity NVM-based RRAM because of their ability to remember former states. They can be easily produced in a crossbar array due to their incredibly small diameters and consistent construction. Aside from their employment in memory systems, memristors have also been used in the logical implementation of functions and interconnections in numerous studies.

Considering memristor technology, the equation (1) shown below proposes the effective memristance of the memristor-based device.

$$M(t) = RON\frac{\omega(t)}{L} + ROFF\left(1 - \frac{\omega(t)}{L}\right) \quad \text{Equation 1}$$

ROFF : Maximum resistance

RON : Minimum resistance

L : thickness of a memristor.

w(t) : thickness of the doped conductive zone as a function of time

The current flowing through the memristor and its physical characteristics are the primary determinants of memristor state change. Because current fluctuates with time, the memristor usually has a non-linear character. This non-linear characteristic can be represented using the window function in the following way, as in equation (2).

$$\frac{dx(t)}{dt} = \frac{\mu_v RoN}{L^2} i(t)F(x(t), P) \quad \text{Equation 2}$$

F(x(t), p) : window function

P : variation of nonlinearity

ROFF : Maximum resistance

i(t) : current flowing through memristor as a function of time

For bigger memristor states, raising p results in a flattened window function [21].

The first memristor developed by HP Labs was titanium dioxide. The memristor is made up of symmetrical oxygen and titanium atom lattices. Because the titanium diode material modifies its resistance in the presence of oxygen, oxygen is employed here. When oxygen gaps or vacancies in the top layer are shifted to the bottom layer, the resistance changes. Charges can be passed through the structure so the memristor can be accessed. In the sandwiched layer, nanowires in the form of crossbars are used. Hence, titanium diode-based memristors are used for the design of the RRAM cells.

Design of 1T1R RRAM Cell

Resistive Random Access Memory (RRAM) based on nonvolatile materials is a viable option in today's memory technology. RRAM's in-memory computing feature allows for accurate read and write operations and can be simply implemented into the CMOS fabrication process. It has a high density and can be 3D-monolithically integrated with other devices. RRAM's low cost and stability are due to its superior performance and efficiency [11].

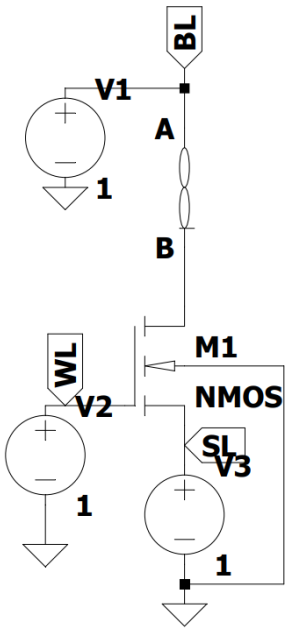

Figure 1. 1T1R RRAM Cell

1T1R (one transistor, one resistor) cell is used to read and write data as an access switch, as shown in Figure 1. In a memristor, the data is stored in the form of resistance. The data is switched between high and low resistance states by the memristor, which is the essential element for resistive switching. The memristor cell operations depend on the duration of access time and the value of the supply voltage applied to WL and SL. The cell is connected to three terminals: the bit line, the source line, and the word line. During read and write operations, the word line is always enabled. To write logic 1, the WL is enabled high and the SL is grounded. The bit line is given some voltage, leading to an increase in voltage, while the resistance drops, resulting in logic 0. For NVM read and write operations, cells in the column share a bit line [12]. The RRAM cell's general architecture is like that of traditional DRAM cells.

Design of 2T1R and 2T2R RRAM Cell

The parameters for 2T1R and 2T2R cell designs are similar to those of 1T1R cell designs. The circuit is set up so that when the word line is switched on, only one of the transistors is turned on and the other is turned off. The rest of the factors are comparable to the resistive RAM's base circuit. The parameters for 2T1R and 2T2R cell designs are similar to those for 1T1R cell designs. The circuit is set up so that when the word line is switched on, only one of the transistors is turned on and the other is turned off. The rest of the factors are comparable to the resistive RAM's base circuit.

The current is regulated during the set operation of an n-type transistor in a 1T1R circuit by direct control of the gate-source voltage. The high voltages that are being investigated will put a strain on the body, such as

I. The bit-cell transistor that has been chosen
II. The neighboring bit-cell selectors have the same BL and WL.

A p-type transistor can be added to the 1T1R bit-cell to solve this problem, resulting in a 2T1R bit-cell. Only the n-type transistors are utilized in this architecture to regulate the current during the set operation (the p-type transistor gate-source voltage is kept zero). The p-type transistor is employed during the reset procedure. Source lines are used to control the set and reset operations. The WLn and WLp Word Lines are used to control the n and p-type transistors separately [22]. The circuit design for the 2T1R cell is illustrated below in Figure 2.

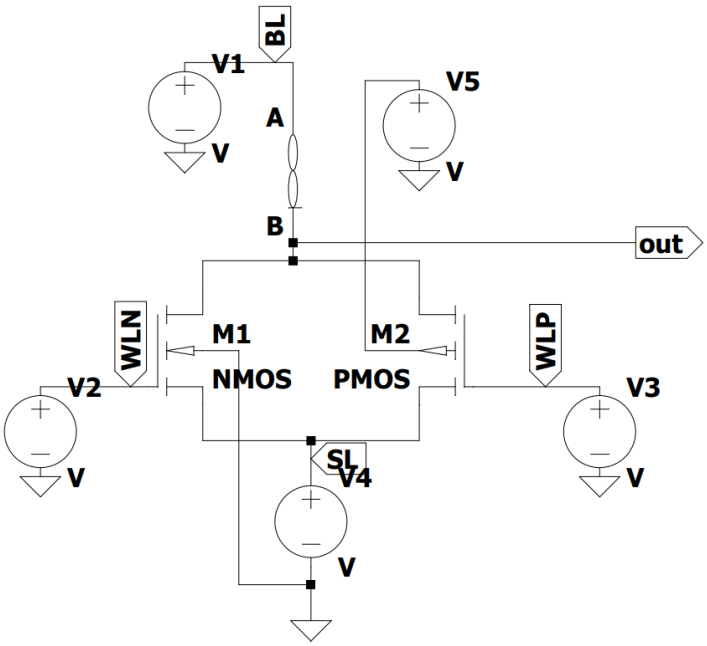

Figure 2. 2T1R RRAM Cell

Here, a design for a 2T2R cell circuit consisting of 2 access Transistors and 2 memristors for storing data is proposed. The proposed circuit design of the 2T2R cell is simulated in Cadence software and compared with the existing SRAM and RRAM cells. Figure 3 below depicts the respective circuit design.

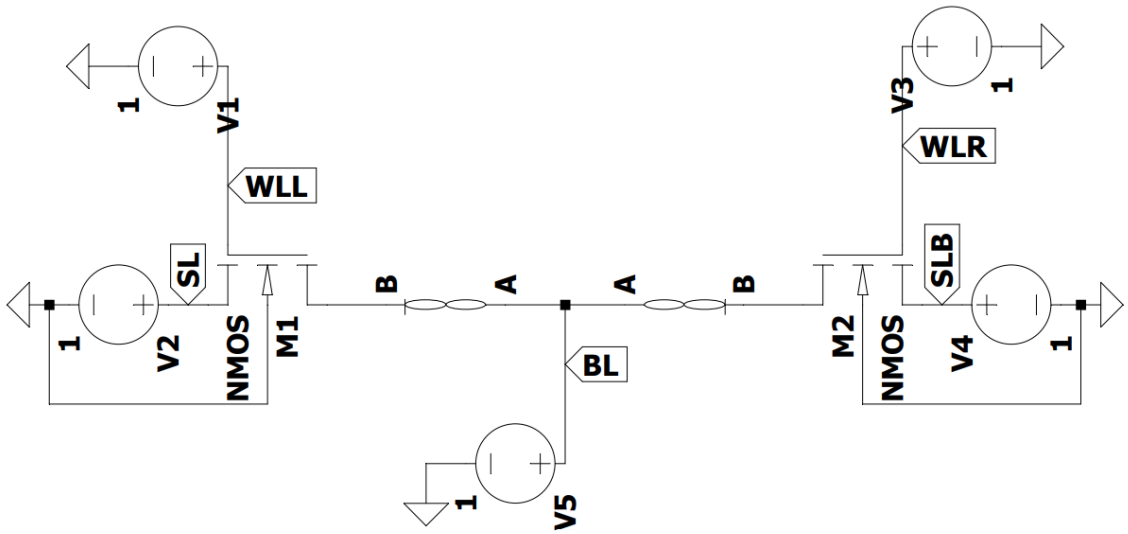

Figure 3. 2T2R Circuit Design

Design of RRAM array

The 4*4 Resistive RAM array is made up of 2T2R structure as shown below in Figure 4.

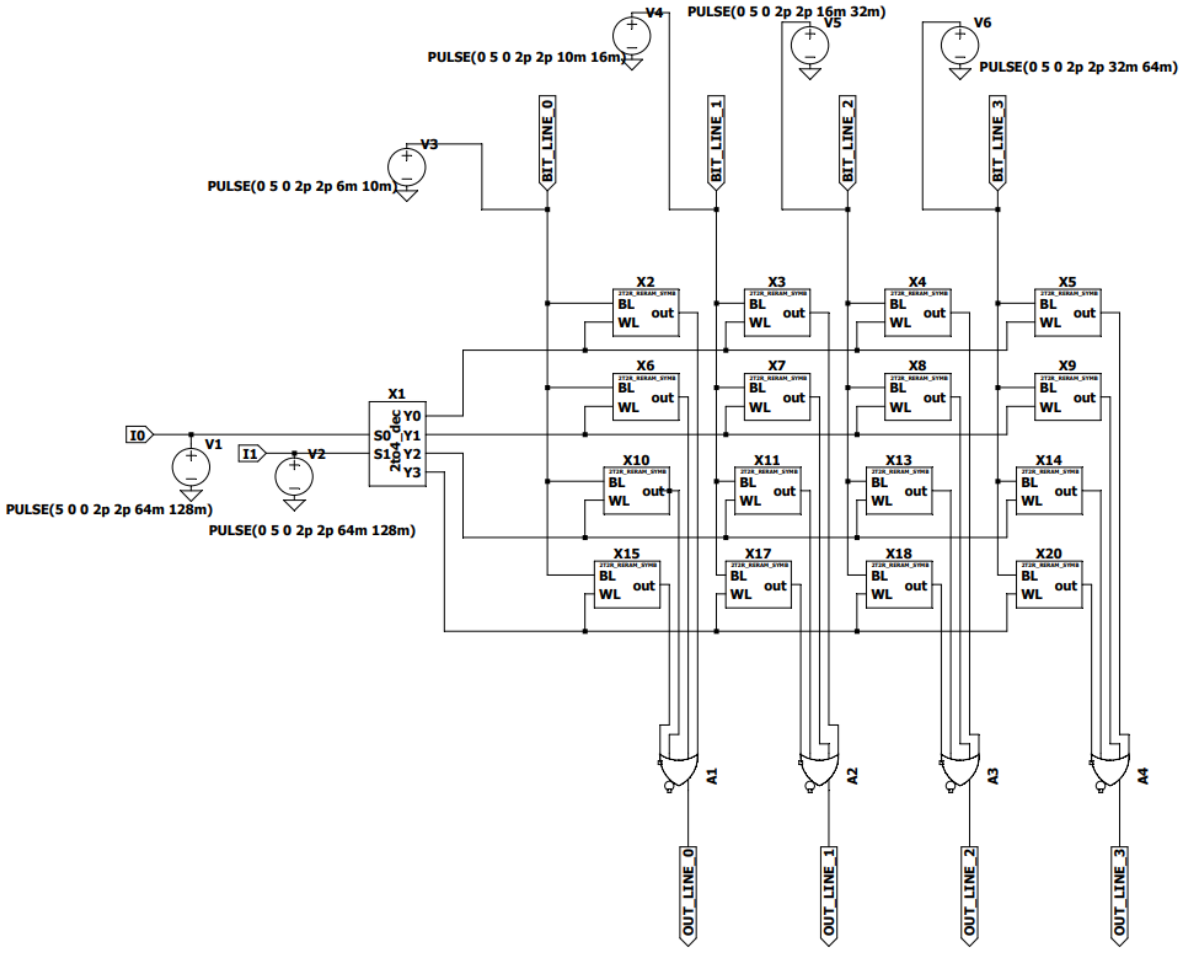

Figure 4. 4*4 Conventional 2T2R Memory Array

The 2T2R ReRAM cell is used as a 4*4 memory array, and the decoder circuit is positioned to choose the appropriate row. The bit line is enabled to pick the column while the matching row is chosen in accordance with the decoder's input. Therefore, the word line will be suitably activated and the required cell will be picked based on the inputs of the decoder and bit line. There are output ports A1, A2, A3, and A4 where you can get the corresponding output. By placing all the three cell structures in the design of RRAM array, the 2T2R structure provided the best results in terms of power, delay, Power Delay Product and Noise Margin.

A 2:4 decoder is used to select any of the word lines from the array. Y0, Y1, Y2, and Y3 are the decoder's outputs, whereas S0 and S1 are the inputs that offer logic "0" and "1" as inputs. Each input combination is used to choose the matching row in accordance with it. For instance, the first row Y0 will be chosen when the input is 00. When input is 01, the second row and subsequently the next rows are selected. To choose an active cell in a column, the bit line is sent as input to the RRAM cell. Writing operations for 0 and 1 are completed in accordance with the values of bit line. In this case, the first active column is chosen using BIT LINE 0, and the OR output is generated at OUT LINE 0 based on the chosen row from the decoder. The same method can be used to obtain the other three outputs. Using 2T2R cells, a 4*4 RRAM array is built, and the power and delay are then determined. Hence a low power memory design of memory array is created using the power and delay reduced efficient ReRAM cells.

As a result, the resistive RAM array can be used in either simple or sophisticated applications to provide the desired output. There are more chances for improving speed and efficiency inside the design because the modified's stability in the circuit has also risen in comparison to conventional design.

PERFORMANCE EVALUATION

The Cadence software was used to develop and simulate the resistive RAM Memory circuit. This work focuses on the read and writes operations of resistive RAM architectures. This section focuses on the observations of the read and the write operations in detail, as well as the inferences that can be derived. The power dissipation of SRAM [14] and RRAM cells is investigated; Delay, PDP, and Noise Margin are also calculated to determine which cell has the best performance and efficiency.

Write Operations for Logic 0 and Logic 1

Logic 0 and 1 can be written in the circuit during write operations. The bit line to pick an active column is grounded while writing logic "0." A voltage is applied to the source line, which is mainly used to reset the entire memory cell or a specific memory cell. During write operations, the word line is always enabled high. Consequently, when the circuit is powered on, the voltage experiences a drop, causing the memristance (memristor resistance) to increase, resulting in a low resistance state, commonly known as logic 1. Figure 5 illustrates the write operation for logic 1 in the 1T1R, 2T1R, and 2T2R cells. By comparing these figures, the voltage curve shows maximum output response in 2T2R cell that means the output impedance offered by 2T2R cell is minimum (Low Resistance State) in logic 1 write operation.

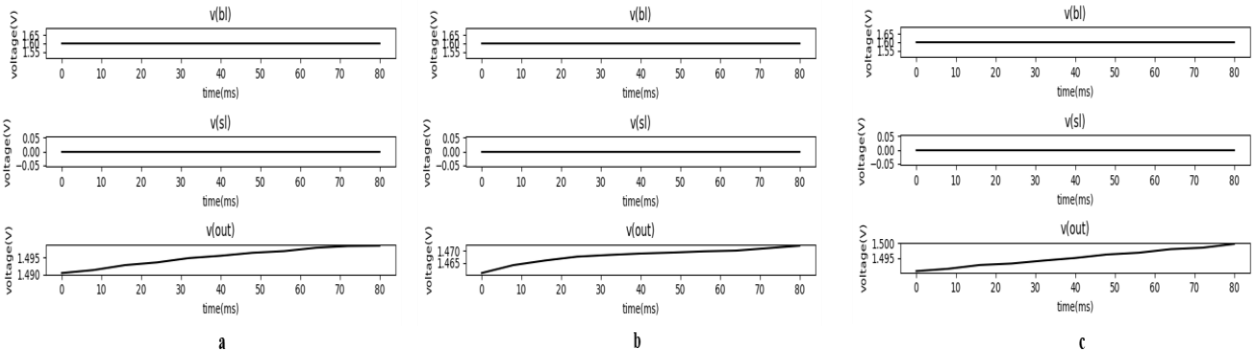

Figure 5. Write 1 Operation in 1T1R, 2T1R and 2T2R Cells

In parallel to write “1” operation, when writing "0," on the other hand, the source line is grounded, the bit line is given a particular voltage, and the Word line is enabled high. As a result, the voltage rises and the memresistance falls, resulting in the High Resistance State (logic 0). Figure 6 shows the output voltage of write operation for logic 0 in various RRAM cells. The minimum output response for logic 0 is also given by 2T2R cell. Since the current flowing through the cell is negligibly small due to the high impedance So writing either ‘1’ or ‘0’ indicates the resistance switching mechanism. It switches between low resistance and high resistance. Therefore, the performance of 2T2R cell is significant and it can be used as a perfect cell to store data in memory operations.

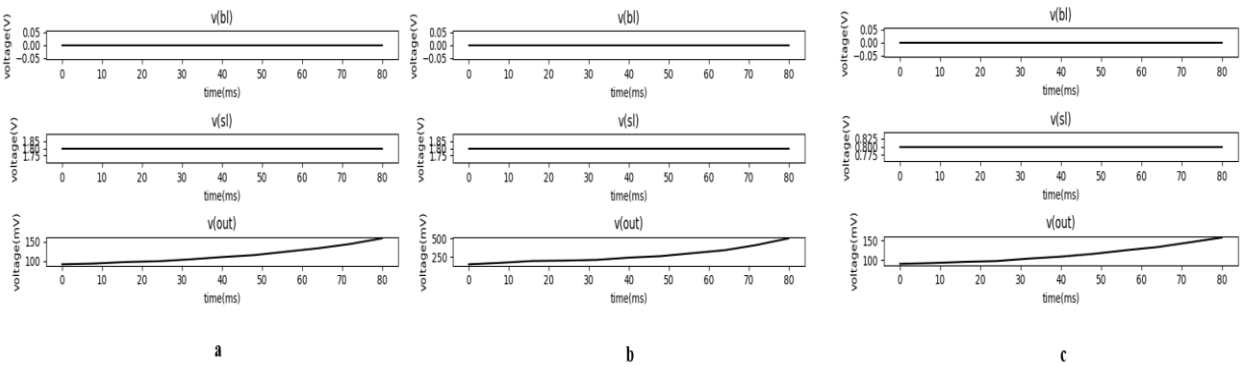

Figure 6. Write 0 Operation in 1T1R, 2T1R and 2T2R Cells

Read Operations for Logic 0 and Logic 1

The information stored in the memristor must be read once the relevant data has been written into the cell. In read operation the word line is enabled and the bit line is pre-charged to half of the supply voltage. For reading logic "0," the word line must be set high for the read operation to take place. The bit line is powered to the desired voltage, so the read voltage is less than half of the threshold voltage, while the source line is grounded. When reading logic "1," on the other hand, the word line is held high and the source line is grounded, as in the previous case, while the bit line is pre-charged to a voltage, which is larger than half of the threshold voltage. The graph is checked in the same way as the write operation for the read operation. The simulations for read operation of logic 0 in 1T1R, 2T1R, and 2T2R cells are shown in the Figure 7.

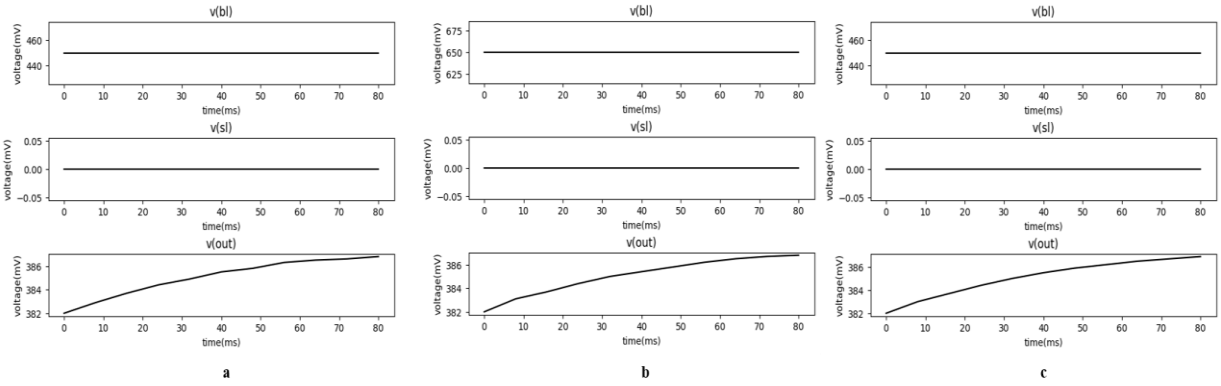

Figure 7. Read 0 Operation in 1T1R, 2T1R and 2T2R Cells

The Figure 8. Shows the Read operation of Logic 1 in various RRAM cells. The 2T2R cell shows a better performance in read operation. It is evaluated by the impedance response of various cell during read operation. The figures 7-8 shows the read operations of logic 0 1nd logic 1 in various RRAM cells such as 1T1R, 2T1R and 2T2R. While reading logic 0 or logic 1, a better simulation response is given by 2T2R cell, the variation in output voltage can be significantly estimate by evaluating the impedance offered by each circuit. Hence the delay, power dissipation and noise margin are calculated further.

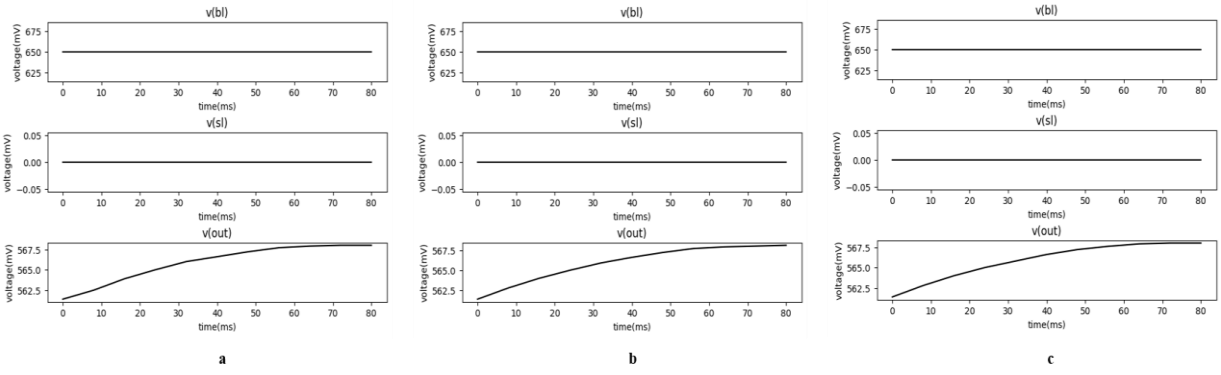

Figure 8. Read 1 Operation in 1T1R, 2T1R and 2T2R Cells

Delay

The read and write delay computations for the three resistive ram circuits are shown in Table 1 below. It can be deduced from the results that as the circuit becomes more complex, the delay increases. This is because of increasing number in access transistors and memristors, the time it takes to write and read values from the appropriate cell grows as well, resulting in a significant delay. The results demonstrate a notable increase in delay characteristics in the proposed 2T2R RRAM model compared to existing RRAM models. The modifications and optimizations implemented in the proposed model contributed to a slight increase in access time but it enhanced overall performance while looking at the other parameters.

Table 1. Delay Computation

Cell Structure (W=0.8u, L=0.5u)	Write 0 (us)	Write 1 (us)	Read 0 (us)	Read 1 (us)
1T1R	93.67	94.45	95.15	95.15
2T1R	94.45	93.67	96.15	96.15
2T2R	**94.67**	**95.45**	**96.15**	**96.15**

Power Dissipation

As the circuit is updated from the base level to the increase in the number of resistors and transistors, the power steadily declines, as indicated in Figure 9. A large reduction in power can be seen when more access transistors and memristors are used in the circuit. As a result, the 2T2R circuit consumes the least amount of power and is used in most data-intensive applications.

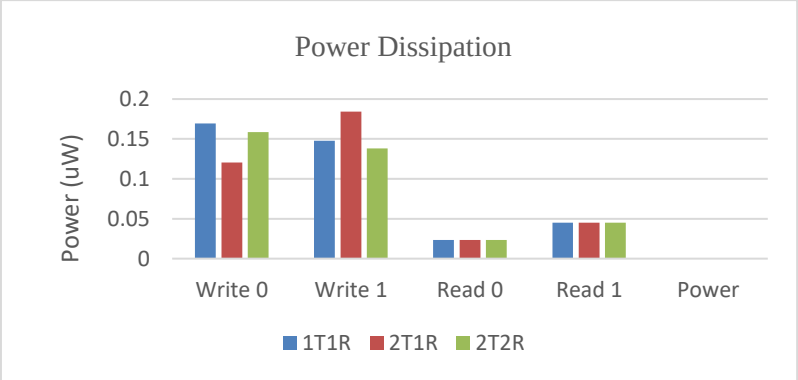

Figure 9. Power Dissipation in 1T1R, 2T1R and 2T2R Cells

Power Delay Product

PDP stands for power delay product, which is defined as the product of power dissipation and propagation delay stated in Nano Joules [15]. It is also known as the average amount of energy used during each switching occurrence. From the PDP values, it is evident that circuits with two transistors and two resistors, or 2T2R, have the smallest power delay product as shown in Table 2 [23]. As a result, most circuits with resistive memories employ the 2T2R structure.

Table 2. PDP of various RRAM Cells

Cell Structure (W=0.8u, L=0.5u)	Power Dissipation (mW)	Delay (us)	PDP (nJ)
1T1R	0.0385	378.42	14.37
2T1R	0.0373	380.42	14.18
2T2R	**0.0365**	**382.42**	**13.95**

Noise Margin and Stability

Noise Margin indicates the operational stability of circuit under any circumstances. The sources of Noise is application specific. It may be power source, noisy electric or magnetic field surroundings, and radiation waves. The designers may consider all the undesired conditions for the circuit development. So that the circuit will be stable in any situation irrespective of noises. Commercially, Stability is the most important need for RRAM memory applications, notwithstanding its diverse capabilities.

The undesired noises may deliberately affect the circuit performance. Therefore, it is essential to design circuits with adequate noise margin. So that it is possible to ensure the desired performance in circuits

under a noisy atmosphere [17]. Commercially, Stability is the most critical need for RRAM memory applications, notwithstanding its diverse capabilities. The primary source of instability is due to the read/write disturbances in the RRAM cells. The term "read disturb" refers to the occurrence in which the state of a selected cell alters after many read operations. To overcome this dilemma, a greater read voltage is desirable for high-speed applications to improve read speed and reduce noise disturbance, which may overwrite the previously stored data. Meanwhile, write disturb happens when the state of an unselected cell changes following a series of write operations on an adjoining cell. Hence, to prevent power consumption, a lower but faster write voltage is desirable.

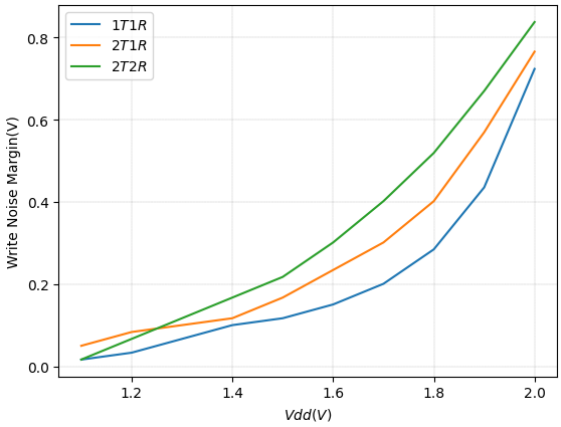

Figure 10. Comparison of Write Noise Margin in 1T1R, 2T1R, 2T2R Cells

The performance of memristors in memory cells is significantly influenced by the power supply value (Vdd). To investigate this effect, a Write Noise Margin (WNM) analysis was conducted on different Vdd levels for each cell in the proposed WNM simulation. Figure 10 illustrates the results, showing that in write mode, higher Vdd levels enhance the immunity of memristor-based cells to noise on Bit Line (BL) and Bit Line Bar (BLB). The 2T2R cells shows the highest WNM. Consequently, the presence of noise on the memristor cell is reduced compared to the 2T1R and 1T1R cell configurations. This noise reduction contributes to the enhanced WNM observed in the 2T2R cell.

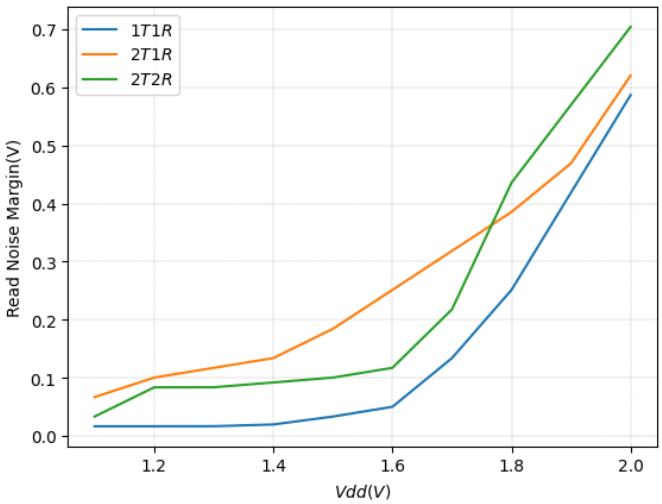

Figure 11. Comparison of Read Noise Margin in 1T1R, 2T1R, 2T2R Cells

In Figure 11, the results of Read Noise Margin (RNM) analysis are presented. For 1T1R, 2T1R and 2T2R cells, the proposed RNM analysis simulated at various power supply levels (Vdd). During read mode, the 2T1R and 2T2R cells exhibit greater tolerance to higher power supply values without damaging the stored data in the memristor device. Therefore, 2T2R cell is significantly more stable than other cells at higher power levels.

CONCLUSION

This research highlights the promising potential of Resistive RAM (RRAM) as a cutting-edge memory technology for future memory device manufacturing. The comparative analysis between advanced 9T SRAM cells and various RRAM cells underscores the superior performance of RRAM in terms of power dissipation, Power-Delay Product (PDP), and noise margin. Particularly, the 2T2R RRAM cell emerges as the most efficient and promising configuration, offering the lowest power consumption and competitive delay characteristics. By utilizing titanium diode-based memristors with a sandwiched structure, the RRAM cells demonstrate their capability to store data in resistance-based memristor cells effectively. Moreover, the integration of the 2T2R cell into a 4x4 memory array showcases its potential practical applicability in RRAM-based applications, providing improved power efficiency and reduced latency compared to SRAM array counterparts. These findings accentuate the importance of RRAM as a leading alternative for memory device design, offering exceptional stability, enhanced read and write performance, and energy efficiency.

As the semiconductor memory landscape continues to evolve, RRAM emerges as a promising candidate that can pave the way for future advancements in non-volatile memory technologies. The 2T2R RRAM cell holds great promise in contributing significantly to the development of high-performance and energy-efficient memory solutions. This research provides valuable insights into the capabilities of RRAM cells and their potential to revolutionize memory technologies, shaping the future of computing and data storage. With ongoing advancements in RRAM fabrication and integration, we envision RRAM to become a key driving force in the ever-expanding realm of memory technology.

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